AMENDMENTS TO THE DRAWINGS:

Responsive to the Examiner's request for clarification, Applicants propose amending drawing Figures 1, 2, 3, 5 and 6, as set forth below.

Regarding Figure 1, Applicants propose adding the identifier "Output" and a lead line to the source of transistor S_2. Support for the amendment and is enabled by the specification and derived from US 2003/0035499 A1.

Regarding Figure 2, Applicants propose adding the identifier "LO" to the gate of the transistor below "FIG. 2". Applicants also propose adding a DCU (Digital Control Unit) that outputs control lines for the switches. Support for the amendment is shown in Figure 4A which shows the DCU. The timed operation of switches to combine and split capacitors is described in the specification. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference.

Regarding Figure 3, Applicants propose adding the identifier "LO" to the gate of the transistor just to the left of the identified "BANK 2". Applicants also propose adding an identifier "TO IFA" and a lead line from the identified to node "C". Applicants further propose adding a DCU (Digital Control Unit) that outputs control lines for the switches. Support for the amendment is shown in Figure 4A which shows the DCU. The timed operation of switches to combine and split capacitors is described in the specification. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference. The output connected to IFA input is described on page 6: line 16 in the specification.

Regarding Figure 5, Applicants propose adding the identifier "LO" to the gate of the transistor just to the left of the identified "BANK 2". Applicants also propose adding the identified "CTL_SAZ" to the gate of the transistor just above the identified "BANK 2". Applicants further propose adding the identifier "CTL_SBZ" to the gate of the transistor

just above the identifier "BANK 1". Applicants yet further propose adding an identifier "TO IFA" and a lead line from the identified to node "B". Applicants also propose adding a "Clock Generation" box with identified output signals CTL_SAZ, CTL_SBZ, CTL_D, and CTL_P. The timed operation of switches to combine and split capacitors is described in the specification on page 6, lines 17-29. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference. The output connected to IFA input is shown also in Figure 4B.

Regarding Figure 6, Applicants propose adding the identifier "LO" to the gate of the transistor just to the left of the identified "BANK 2". Applicants also propose adding the identified "CTL_SAZ" to the gate of the transistor just above the identified "BANK 2". Applicants further propose adding the identifier "CTL_SBZ" to the gate of the transistor just above the identifier "BANK 1". Applicants yet further propose adding an identifier "TO IFA" and a lead line from the identified to node "B". Applicants also propose adding a "Clock Generation" box with identified output signals CTL_SAZ, CTL_SBZ, CTL_D, and CTL_P. The timed operation of switches to combine and split capacitors is described in the specification on page 6, lines 17-29. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference. The output connected to IFA input is shown also in Figure 4B.

Applicants respectfully request approval.

REMARKS/ARGUMENT

1) Claims 1-33 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner rejects claims 1-33 mainly based on the fact that the subject matter is unclear to him. Applicants propose amending Figures 2, 3, 5 and 6 and clarify claims 1, 2, 3, 6, 7, 8, 9, 10, 12, 22, 23, 25, 26, 27, 28, 29, 30 and 32 as set forth below.

A detailed operation of Figure 1, which is the basis for Figures 2—6, is explained in U.S. Pub. No. US 2003/0035499 A1, which is incorporated by reference in its entirety ([paragraph 0024]). In this response Applicants will clarify the claims by pointing to the subject matter referred to in order to improve understanding of the material.

Claim 1: Examiner states that it is unclear how the filters can be "configured" on line 2. The same is true for Claim 21.

Applicants' response: In Claim 1, "configured" refers to setting up the topology (or configuration of) rotating and fixed capacitors as shown in the figures and as explained in the specification and in U.S. Pub. No. US 2003/0035499 A1, which is incorporated by reference in its entirety. If set as described in figure 2, the output of CB1 is connected to the input of IFA. The first IIR filter stage of CH and CR1 is described in [0025]. The second IIR filter stage of CR1 and CB1 is described in [0026]. If set as described in figure 3, the output of CB3 is connected to the input of IFA. If set or configured as shown in figure 4, the output of CB is connected to the input of the voltage follower (which is an IF amplifier). When configured as shown in figures 5 and 6, the output of CB2 is connected to the input of the IFA. The specification describes different configurations to obtain

cascaded passive IIR filter response using combination of discrete-time ANALOG data samples. The specification describes obtaining various orders of filtering and the effects or resetting or not resetting charge on the rotating capacitors. The same meaning is inferred in claim 21.

Claim 2: Examiner states it is unclear what the "high order filter devoid of amplifiers" on line 3 is and how the filters and the means for direct sampling on line 1 can implement the high filter devoice of amplifiers and how this limitation is read on the preferred embodiment or seen on the drawings. The same is true for claims 6, 22 and 26.

Applicants' response: Regarding the recitation, "a high order filter devoid of amplifiers", the cascaded stages do not have amplifiers between them. Looking at figure 2, 3, 5 and 6, it is quite apparent that higher than single order of IIR filtering is achievable with the presented invention **without using inter-stage amplifiers**. Inter-stage amplifiers are **always needed to develop high order analog filters** in order to isolate the impact of loading. The current invention provides a means of obtaining high order IIR filters **without using any amplifiers**. Equations (25) and (27) drives this point home for second order IIR filter obtained without any amplifier separating the rotating and fixed capacitors. The "PIIR" stage, thus obtained can be cascaded without any separation with the amplifiers. One could place amplifiers between a cascade of multiple PIIR stages as shown in figure 4. The same is true for claims 6, 22 and 26.

Claim 3: Examiner states it is unclear how the recitation "means ... mixer" on lines 1-2 is read on the preferred embodiment. Insofar as understood, no such means is seen on the drawings . The same is true for claims 23 and 25.

Applicants' response: Regarding the recitation "mixer", Figure 4 shows the mixing operation quite clearly. The LO connected to the input sampling capacitor mixes the RF signal down to baseband frequency as shown in figure 4. For improving the clarity of the presentation, the figures show the LO connected to the input sampling switch. Following the down-conversion, PIIR filter stages perform high-order IIR filtering without using inter-stage IF amplifiers. This is described in great detail in US 2003/0035499 A1 and is referred to in the specification on page 5: line 1-9 and on page 16: lines 4-26. The same is true for claims 23 and 25.

Claim 7: Examiner states it is unclear how the filters can create a unit-directional flow of information, signal or charge, what they are and where they come from. The same is true for Claim 27.

Applicants' response: Regarding the recitation "uni-directional flow of information", this is described in [0027]. The charge comes from the RF current signal, is down-converted, sampled, processed by PIIR filter stages and handed off to an IF amplifier for further processing. The output of the final capacitor is read-out for further post-processing as shown in all figures.

This is further described on page 5: lines 11-30 and page 6: lines 1-11 (of the original application). The issue described is that input RF current is down-converted by LO through the input sampling switch shown in figure 2, 3, 4, 5 and 6 and integrated on CH+CR1. There are two banks of CR1. As CR1 is combined with CB1, the charge it holds is combined with the charge that pre-exists on CB1. When they are split again, each take on a new charge that is proportional to its size. In the next operation cycle, CR1+CH integrate the RF input current again and in doing so, the charge that pre-exists on CR1 is combined with CH creating a feedback from CB1 to CH. This is described on page 10:

lines 7-11. To break this feedback, CR1 is RESET (meaning that the charge that exists on it is not forced to zero) every time prior to recombining with CH. Then there is no feedback from CB1 to CH and the charge flow is only from CH to CB1.
Now extending this to figure 3, of CR1 and CR2 are reset each time before the are combined back with CH and CB1, respectively, there will be no feedback from a later stage to an earlier stage, thereby creating a direction of signal flow from left to right only and no signal flow from right to left due to feedback.

Claim 8: Examiner states that the description of the present invention is incomplete because the capacitors and the capacitor banks are not connected to anything. Thus, the claimed capacitor and the capacitor banks may not perform the recited function. The same is true for Claim 28.

Applicants' response: The final output of the PIIR stages is connected to an IF amplifier. It is thereby converted from analog to digital and the information it carries is detected after digital post-processing. This is explained in US 2003/0035499 A1. One objective of the present invention is to show how to obtain a higher order IIR filter by cascading several IIR filter stages without requiring amplifiers in between the stages. The same is true for claim 28.

Claim 9: Examiner states that it is unclear how the capacitor can be "reset" since no means for performing the resetting function is recited in the claim. The same is true for Claim 29.

Applicants' response: The function of "resetting" the capacitor is shown in figure 6 and explained on page 8: lines 23-28, page 9: lines 1-10, 28-31, page 10: lines 1-11. The same is true for claim 29.

Claim 10: Examiner states that it is unclear how the recitation "comparator" and "negative feedback loop" is read on the preferred embodiment. Insofar as understood, no such loop and comparator are seen on the drawings. The same is true for claim 30.

Applicants' response: Figure 14 shows a generic sigma-delta A/D converter that is constructed using a loop filter followed by a comparator in a negative feedback loop. Claim 10 applies to the application of the cascaded PIIR filter based design of the loop filter part of the A/D converter. The cascaded IIR filter may be used to construct the loop filter of a sigma-delta A/D converter. The same is true for claim 32. This is also emphasized on page 2 of the specification in lines 8-13 for other applications of this invention also.

Claim 12: Examiner states that it is unclear how the RF input signal can be minus a negative feedback signal since no means for performing the subtracting function is recited in the claim. The same is true for claim 32.

Applicants' response: Figure 14 shows a generic sigma-delta A/D converter that is constructed using a loop filter followed by a coparator in a negative feedback loop. Claim 12 is related to the application of the cascaded PIIR filter based design of the loop filter part of the A/D converter when the input signal is an RF signal which is down-converted by the LO and consequently becomes a baseband signal. The down-conversion is shown by the mixer switch driven by "LO" in several figures in the specification. The cascaded

IIR filter may be used to construct the loop filter of a sigma-delta A/D converter. The same is true for Claim 32. This is also emphasized on page 2 of the specification in lines 8-13 for other application of this invention.

The subtraction operation is performed by adding a negative contribution. Referring to Figure 14, the subtractor sign is realized by adding a negative current or charge packet 406 generated by the DAC. It is straightforward in practice to generate a negative contribution by inverting the current direction, swapping the positive and negative feeds of a differential signal or inverting the digital word input to the DAC. These methods are well known in the art. The details are presented in US 2003/0035499 (Figures 10, 11a, 16a, 16b, 20), which is incorporated in its entirety.

2) Claims 1-3, 6-7, 21-23 and 26-27 stand rejected under 35 U.S.C. 102(b) as being anticipated by Simon et al (GB 2230627). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1-3, 6-7, 21-23 and 26-27 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites a discrete time **analog** filter comprising **a cascade of single pole IIR filters configured** to generate an output signal in response to an input signal.

Independent Claim 21 requires and positively recites a receiver front-end comprising **a cascade of single pole IIR filters configured** to generate an output signal in response to an input signal.

In contrast, Simon et. al (GB 2230627) discloses a recursive processor (like a microprocessor) for DIGITAL infinite impulse response (IIR) filters. It would be obvious to anyone skilled in art that digital implementations of filters do not teach analog implementations, since digital implementations deal with abstraction of information as bits and words and are based on a uni-directional flow of information, while analog filters implementation deal with manipulation of analog quantities with passive and active elements. The present invention provides a solution to an analog problem of implementing high order passive analog IIR filter embedding a mixer. The detailed description of the mixer operation is presented in U.S. Pub. No. US 2003/0035499 A1. As such, Simon et al fails to teach or suggest all of the limitations of Claims 1 and 21.

Claims 2-3, 6-7, 22-23 and 26-27 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

3) Claims 1, 6, 21 and 26 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al (US 5,732,002). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1, 6, 21 and 26 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites a discrete time **analog** filter comprising **a cascade of single pole IIR filters configured** to generate an output signal in response to an input signal.

Independent Claim 21 requires and positively recites a receiver front-end comprising **a cascade of single pole IIR filters configured** to generate an output signal in response to an input signal.

In contrast, Lee also shows a digital filter implementation while the present invention relates to an analog filter implementation. The building blocks in one are entirely different from the building blocks in the other. In digital filters, there is no concept of "impedance" or "load", which, in an analog filter can completely change the properties (transfer function) of the filter. This phenomenon is further emphasized in the context of novelty. While, arguendo, it may be obvious in the field of digital design to cascade digital single-stage IIR filters for the benefit of stronger overall filtering, since the signal flow there is strictly uni-directional with no effects of the next stage on the previous

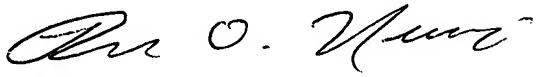
stage, similar configuration in analog domain does not work. In analog domain, on the other hand, the signal flow is all-directional so that Kirchoff's laws are satisfied. Connecting a single-stage IIR filter with another one changes the loading environment in both stages to the point where the desired higher-order transfer function can rarely be obtained.

The common method of achieving higher-order filtering in analog domain is to isolate the stages with active elements, such as amplifiers. The Examiner has cited no prior art that shows how to obtain higher order IIR filtering without having amplifiers or active stages in the circuit. As such, Simon et al fails to teach or suggest all of the limitations of Claims 1 and 21.

Claims 6 and 26 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Applicants appreciate the Examiner's indication that Claims 4-5, 8-20, 24-25 and 28-40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in the Office action and to include the limitations of the base claim and any intervening claims, but Applicants believe in light of the above arguments that Claims 1-40 are allowable in their present form. Accordingly, Applicants respectfully request allowance of the application as the earliest possible date.

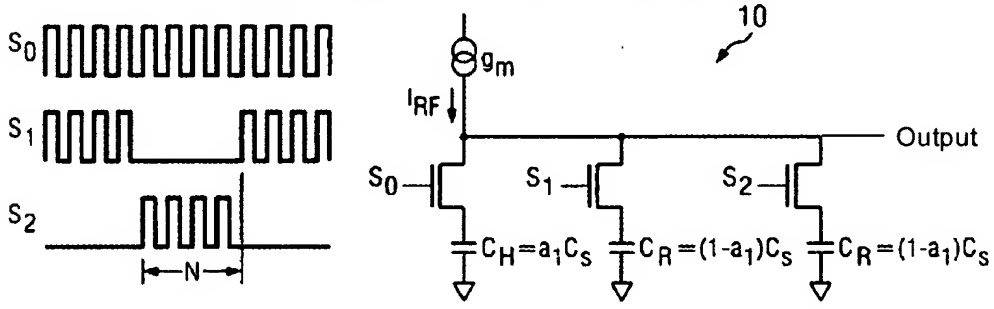
Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418

FIG. 1



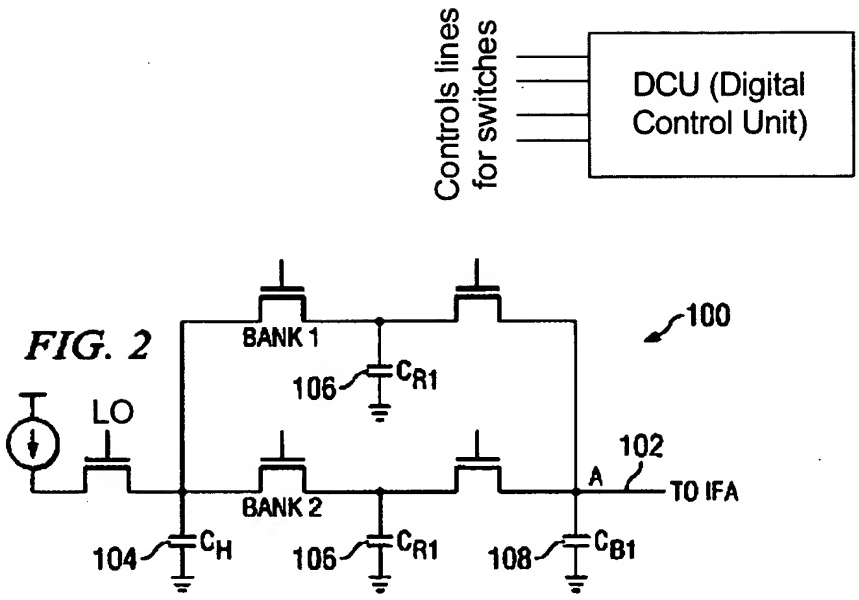

Controls lines for switches
DCU (Digital Control Unit)
100
BANK 1
106
C_{R1}
LO
102
A
TO IFA
BANK 2
104
C_H
106
C_{R1}
108
C_{B1}

FIG. 2

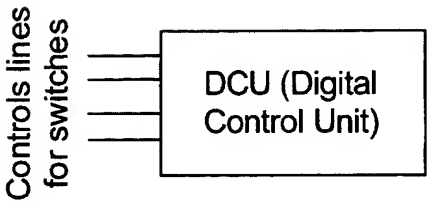
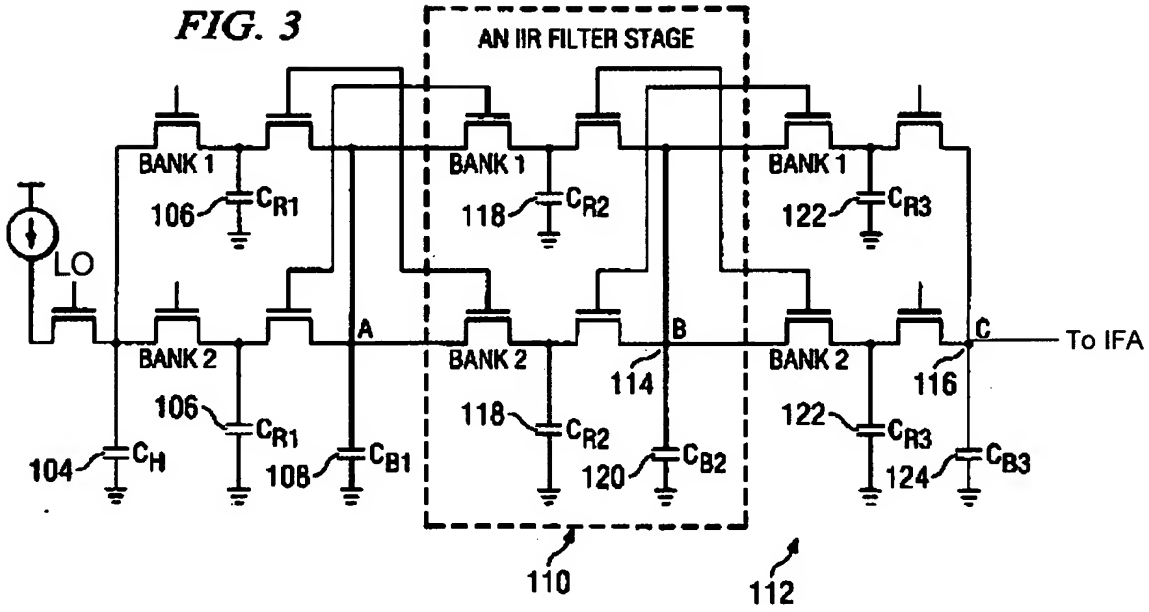

Controls lines for switches
DCU (Digital Control Unit)

FIG. 3


AN IIR FILTER STAGE
BANK 1
BANK 2
LO
106
C_{R1}
118
C_{R2}
122
C_{R3}
A
B
C
To IFA
104
C_H
108
C_{B1}
120
C_{B2}
124
C_{B3}
114
116
110
112

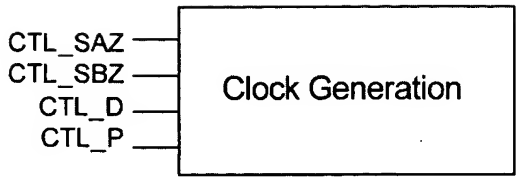
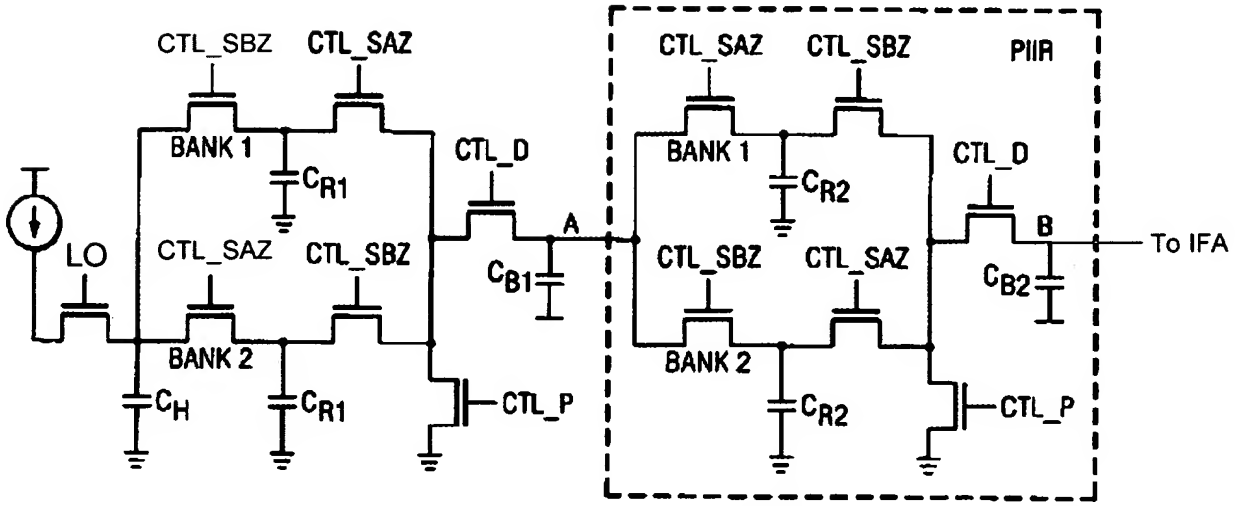

CTL_SAZ
CTL_SBZ
CTL_D
CTL_P
Clock Generation

FIG. 5


CTL_SBZ
CTL_SAZ
BANK 1
C_{R1}
CTL_D
A
LO
CTL_SAZ
CTL_SBZ
C_{B1}
BANK 2
C_H
C_{R1}
CTL_P
CTL_SAZ
CTL_SBZ
PIIR
BANK 1
C_{R2}
CTL_D
B
To IFA
CTL_SBZ
CTL_SAZ
C_{B2}
BANK 2
C_{R2}
CTL_P

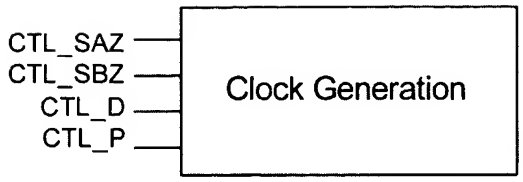
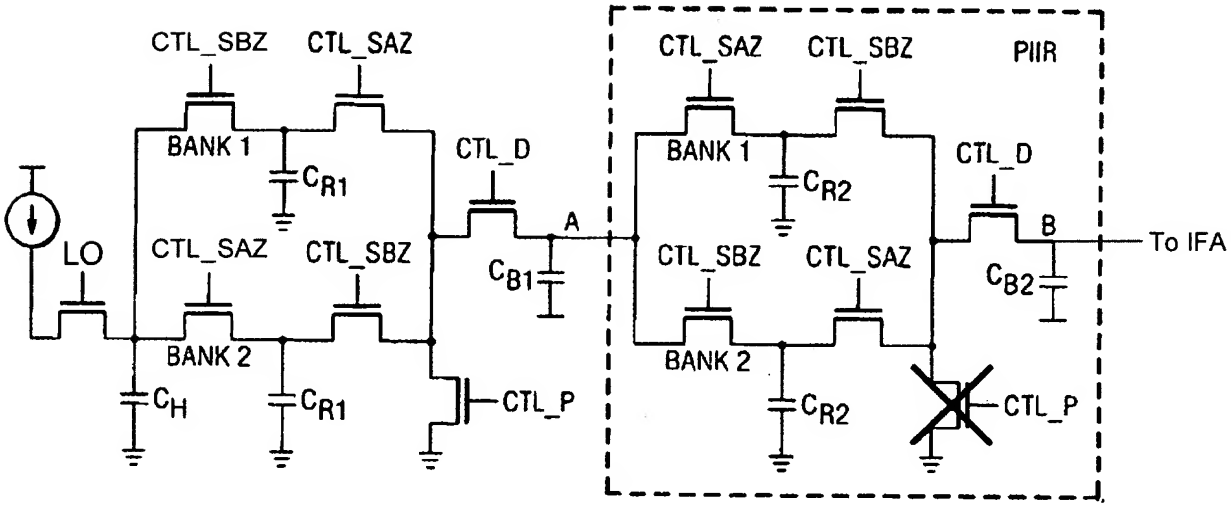

CTL_SAZ
CTL_SBZ
CTL_D
CTL_P
Clock Generation

FIG. 6


CTL_SBZ
CTL_SAZ
BANK 1
C_{R1}
CTL_D
A
LO
CTL_SAZ
CTL_SBZ
C_{B1}
BANK 2
C_H
C_{R1}
CTL_P
CTL_SAZ
CTL_SBZ
PIIR
BANK 1
C_{R2}
CTL_D
B
To IFA
CTL_SBZ
CTL_SAZ
C_{B2}
BANK 2
C_{R2}
CTL_P